CLAIMS

What is claimed is:

1. A method for nested control flow, the method comprising:

setting a context bit to at least one of: a first state and a second state

receiving a first instruction having a plurality of extra bits;

determining whether to read the context bit based on the plurality of extra bits; and

if the context bit is read, executing the instruction when the context bit is in the first state.

2. The method of claim 1 further comprising:

upon the executing of the first instruction, maintaining a counter value wherein the counter value indicates a nesting depth of context bits that are set to a second state.

3. The method of claim 2 wherein the counter is stored in a non-dedicated memory device.

4. The method of claim 3 wherein the non-dedicated memory device is a general purpose register.

5. The method of claim 2 further comprising:

prior to setting the context bit, resetting the counter value.

6. The method of claim 2 further comprising:

receiving a second instruction having a plurality of extra bits;

determining whether to read the context bit based on the plurality of extra bits;

if the context bit is read, executing the instruction when the context bit is in the first state; and

upon executing the second instruction, maintaining the counter.

7. The method of claim 6 further comprising:

terminating a computation processing using the counter.

8. An apparatus for nested control flow, the apparatus comprising:

a processor having a context bit;

a first memory device storing a plurality of instructions, wherein each of the plurality of instructions includes a plurality of extra bits, the processor operative to execute the plurality of instructions; and

a second memory device operably coupled to the processor, the memory device receiving an incrementing counter instruction upon the execution of one of the plurality of instructions.

9. The apparatus of claim 8 further comprising:

a context bit memory device capable of storing the context bit.

10. The apparatus of claim 8 wherein the second memory device is a general purpose register.

11. The apparatus of claim 8 wherein the processor receives a first instruction having a plurality of extra bits from the memory and the processor determines whether to read the context bit based on the plurality of extra bits.

12. The apparatus of claim 11 wherein the processor executes the first instruction when the context bit is read and is in a first state and the processor maintaining a counter value wherein the counter value indicates a nesting depth of context bits that are set to a second state, in response to the incrementing counter instruction.

13. The apparatus of claim 12 wherein the process receives a second instruction having a plurality of extra bits from the memory and the processor determines whether to read the context bit based on the plurality of extra bits and if the context bit is read, executing the

second instruction when the context bit is in a first state and incrementing the counter bit in response to the incrementing counter instruction.

14. A graphics processing device comprising:

a plurality of arithmetic logic units, each of the plurality of arithmetic logic units having a context bit memory device capable of storing a context bit;

a first memory device storing a plurality of instructions, wherein each of the plurality of instructions includes a plurality of extra bits, the arithmetic logic units operative to execute the plurality of instructions; and

a second memory device operably coupled to the processor, the second memory device receiving an incrementing counter instruction upon the execution of one of the plurality of instructions.

15. The graphics processing device of claim 14 wherein the second memory device is a general purpose register.

16. The graphics processing device of claim 14 wherein each of the plurality of arithmetic logic units receive at least one of the plurality of instructions and the arithmetic logic units determine whether to read the context bit based on the plurality of extra bits.

17. The graphics processing device of claim 16 wherein the plurality of arithmetic logic units execute the instructions when the context bit is read and is in a first state and maintaining a counter value wherein the counter value indicates a nesting depth of context bits that are set to a second state, in response to the incrementing counter instruction.

18. The graphics processing device of claim 17 wherein the plurality of arithmetic logic units are operative to terminate a processing chain utilizing the context bit stored in the second memory device.

19. A method for nested control flow, the method comprising:

setting a context bit to at least one of: a first state and a second state

receiving a first instruction having a plurality of extra bits;

determining whether to read the context bit based on the plurality of extra bits;

if the context bit is read, executing the instruction when the context bit is in the first state; and

upon the executing of the first instruction, maintaining a counter value wherein the counter value indicates a nesting depth of context bits that are set to a second state. in a general purpose register.

20. The method of claim 19 further comprising:

receiving a second instruction having a plurality of extra bits;

determining whether to read the context bit based on the plurality of extra bits;

if the context bit is read, executing the instruction when the context bit is in the first state; and

upon executing the second instruction, incrementing the counter.

21. The method of claim 20 further comprising:

terminating a computation processing using the counter.